RR1X2 Digital Latch Sensor Series

PRODUCT QUALIFICATION REPORT

April 3, 2020

66 Whitecap Drive, North Kingstown, RI 02852 / Tel: +1-401-943-2686, Fax: +1-401-942-0920

Summary

This report documents the qualification and test results for Coto Technology's RR1X2 series of Sensor products.

The digital latch sensors are fabricated using Coto Technology's next generation TMR process and assembled in industry standard packages such as SOT23 and LGA-4.

All of the environmental tests were performed at an accredited independent testing lab.

In total, 3,030 devices were tested with a variety of qualification stress tests under various test conditions. There were zero failures. The RR1X2 series of Sensor products has passed all of the reliability tests and is fully qualified.

Reference Documents

JESD47I:	Stress-Test-Driven Qualification of Integrated Circuits
JESD22-A113:	Preconditioning MLS1, MSL3
JESD22-A103:	High Temperature Storage Life (HTSL)
JESD22-A104:	Temperature Cycling
JESD22-A108:	Temperature, Bias, and Operating Life (HTOL)
JESD22-A118:	Unbiased HAST
JESD22-A110:	Biased HAST
JEDEC-JS001-2014:	ESD
JESD78:	Latch Up

Table of Contents

1. Product Tested

The TMR Digital Latch/Analog sensor products are fabricated using Coto Technology's next generation TMR process and assembled in industry standard packages.

All tests are performed by an accredited independent testing lab.

In total, 3,030 devices were stressed with a variety of qualification tests under various test conditions. Of the devices tested, there were zero failures during qualification testing.

2. Definition of Qualification

The RR1X2 series of products are defined as products meeting all of the following criteria:

- A single TMR process technology (TMR = Tunneling Magnetoresistance)
- The same design rules and process technology.

3. Qualification Test Plan

The product qualification test plan is outlined in Table 1. This plan is based on the guidelines of the JESD47I, *Stress-Test-Driven Qualification of Integrated Circuits*, published by JEDEC Solid State Technology Association.

Table 1 – List of Qualification Tests

Test	Stress	Duration	Sample Size
Parametric Tests	Evaluate Data Sheet Spec. @ +25°C	N/A	All Devices Used for Qualification
Pre-Conditioning	Thermal, Mechanical for Package Integrity: • SOT23	MSL1	52 lots (2,530 units)
Pre-Conditioning	Thermal, Mechanical for Package Integrity: • LGA	MSL3	1 lots (500 units)
Temperature Cycling	Thermal Mechanical	-55°C and +125°C @ 3 cycles/hr, 1,000 cycles	6 lots (462 units)
Unbiased HAST(1)	Thermal Moisture	+130°C, RH 85%, 96 hours	6 lots (462 units)
Biased HAST	Bias, Thermal Moisture	V_{DD} = 4.0V & 5.8V @ +130°C, RH 85%, 96 hours	6 lots (462 units)
HTOL(2)	Bias, Thermal	1,000 hours (See Bias Conditions in Table 5 of Section 6.5)	6 lots (462 units)
High Temperature Storage	Thermal, Material Relaxation	1,000 hours (See Static Bake Conditions in Table 6 of Section 6.6)	6 lots (462 units)
Latch-Up	Electrical	JESD78 (±200 mA)	2 lots
ESD	Human Body Model	JEDEC-JS001-2014	2 lots

(1) HAST – Highly accelerated temperature/humidity stress test
(2) HTOL – High temperature operation life

4. Sampling Plan

Random samples were selected for product qualification as shown in Table 1. Sample size meets or exceeds the number of samples recommended by JESD47K standard. Seventy-seven (77) sample units per lot were used for each stress test with 5% LTPD.

5. Failure Criteria

A device failure is defined as a condition in which a stressed device can no longer meet its datasheet specifications or it has consequential physical damage attributed to an environmental test.

6. Summary of Qualification Test Results

A summary of qualification test results is provided in following sections.

6.1. Pre-Conditioning

A total of 2,530 devices were pre-conditioned using JESD22-A113 MSL level 1 and 500 procedures using MSL level 3 procedures. Preconditioning is performed on samples before they are subjected to package-related stress tests. The samples were exposed to thermally stressful conditions equivalent to thermal conditions experienced by units during board soldering.

Table 1.2 – Pre-conditioning Test Results

Wafer Lot	MSL Level	Sample Size	Devices Failed	Test Outcome
T851458, T850891, T968658, T970247, T968568	1	2,530	0	Pass
T970247.13	3	500	0	Pass

All parts have passed the Pre-conditioning.

6.2. *Temperature Cycling*

A total of 462 devices were tested with temperature cycling. Temperature cycling stresses devices between -55°C to +125°C at 3 cycles per hour for 1,000 cycles. This test is used for the analysis of package performance.

Table 2 – Temperature Cycling Results

Wafer Lot	# of Cycles	Sample Size	Devices Failed	Test Outcome
T851458	1000	77	0	Pass
T850891	1000	77	0	Pass
T968658	1000	77	0	Pass
T970247	1000	77	0	Pass
T968568	1000	77	0	Pass
T970247.13	1000	77	0	Pass

All parts have passed the Temperature Cycling test.

6.3. *Unbiased HAST Test (Highly Accelerated Temperature/Humidity Stress Test)*

A total 462 devices were tested for HAST. The HAST is done at +130°C and 85% relative humidity for 96 hours. This test is used for the analysis of package performance.

Table 3 – Unbiased HAST Results

Wafer Lot	Test Duration	Sample Size	Devices Failed	Test Outcome
T851458	96 hours	77	0	Pass
T850891	96 hours	77	0	Pass

Wafer Lot	Test Duration	Sample Size	Devices Failed	Test Outcome
T968658	96 hours	77	0	Pass
T970247	96 hours	77	0	Pass
T968568	96 hours	77	0	Pass
T970247.13	96 hours	77	0	Pass

All parts have passed the unbiased HAST test.

6.4. Biased HAST Test (Biased Highly Accelerated Stress Test)

A total of 462 devices were tested on biased HAST. The HAST is done at +130°C and 85% relative humidity under lot numbers T851458 and T850891 at 4.0 V and lot numbers T968658, T970247, T970247.13 and T968568 at 5.8 V bias for 96 hours. This test is used for analysis of package performance under extreme operating conditions.

Table 4 – Biased HAST Results

Wafer Lot	Test Duration	Sample Size	Devices Failed	Test Outcome
T851458	96 hours	77	0	Pass
T850891	96 hours	77	0	Pass
T968658	96 hours	77	0	Pass
T970247	96 hours	77	0	Pass
T968568	96 hours	77	0	Pass
T970247.13	96 hours	77	0	Pass

All parts have passed the biased HAST test.

6.5.1 HTOL Test (High Temperature Operation Life Test)

A total of 462 devices were tested HTOL. This test is used in the analysis of lifetime of the device under extreme operating conditions.

Table 5 – HTOL Results

Wafer Lot	Sample Size	# of Hours	Bias Condition	Devices Failed	Test Outcome
T850891	77	1000	5.5 V @ +150°C	0	Pass
T851458	77	1000	3.7 V @ +150°C	0	Pass
T968658	77	1000	5.8 V @ +160°C	0	Pass
T970247	77	1000	5.8 V @ +160°C	0	Pass
T968568	77	1000	5.8 V @ +160°C	0	Pass
T970247.13	77	500	5.8 V @ +125°C	0	Pass

A total of 385 parts have passed 1,000 hours of HTOL test. Wafer lot number T970247.13 passed 500 hours. Parts from lot number T970247.13 are under test for a cumulative of 1,000 hours.

6.5.2 Early Life Failure Rate

Total of 776 units of various lots were stressed with high temperature life stress conditions (5.8 V, +160°C) for 168 hours and 150 units at 5.5 V at +150°C. These units all passed the electrical test following the stress tests; there were no failures.

6.6. High Temperature Storage Test

A total of 462 devices were tested on high temperature storage. This test is used for analysis of device performance.

Table 6 – High Temperature Storage Results

Wafer Lot	Sample Size	# of Hours	Bake Temperature	Devices Failed	Test Outcome
T850891	77	1000	+150°C	0	Pass
T851458	77	1000	+150°C	0	Pass
T968658	77	1000	+150°C	0	Pass
T970247	77	1000	+150°C	0	Pass
T968568	77	1000	+150°C	0	Pass
T970247.13	77	1000	+150°C	0	Pass

All parts have passed the high temperature storage test.

6.7. ESD (HBM)

Human Body Model test was performed on a number of samples from two (2) lots of RR1X2 series to characterize the susceptibility of devices to damage from electrostatic discharge (ESD) induced by human handling. The resulting data did not show any notable change due to ESD. The products are qualified for ±4 kV per JEDEC-JS001-2014.

6.8. Latch-up (LU)

The latch-up characterization was successfully completed on samples from two (2) lots of the RR1X2 series using excessive current flow between the power supply and ground as well as output to power pin and to ground. The products are qualified per JESD78.

7. Conclusion

The RR1X2 series of products were tested as described in this report. All devices were electrically tested, and sample units were magnetically tested per the datasheet's specifications. The RR1X2 series is qualified per JEDEC standards.

Revision History:

Revision	Date	Description
0.0	8/15/2019	Initial Release – Pre-qualification Report
0.1	12/20/2019	Added Partial data Lot# T968658 & T970247
0.2	4/3/2020	Full Qual Report. Added 3 SOT23 & 1 LGA lot data

