Qualification Test Plan

The product qualification test plan is outlined in Table 1. This plan is based on the guidelines of the JESD47I, *Stress-Test-Driven Qualification of Integrated Circuits*, published by JEDEC Solid State Technology Association.

Table 1 – List of Qualification Tests

Test	Stress	Duration	Sample Size
Parametric Tests	Evaluate Data Sheet Spec. @ +25°C	N/A	All Devices Used for Qualification
Pre-Conditioning	Thermal, Mechanical for Package Integrity: • SOT23	MSL1	52 lots (2,530 units)
Pre-Conditioning	Thermal, Mechanical for Package Integrity: • LGA	MSL3	1 lots (500 units)
Temperature Cycling	Thermal Mechanical	-55°C and +125°C @ 3 cycles/hr, 1,000 cycles	6 lots (462 units)
Unbiased HAST(1)	Thermal Moisture	+130°C, RH 85%, 96 hours	6 lots (462 units)
Biased HAST	Bias, Thermal Moisture	V_{DD} = 4.0V & 5.8V @ +130°C, RH 85%, 96 hours	6 lots (462 units)
HTOL(2)	Bias, Thermal	1,000 hours (See Bias Conditions in Table 5 of Section 6.5)	6 lots (462 units)
High Temperature Storage	Thermal, Material Relaxation	1,000 hours (See Static Bake Conditions in Table 6 of Section 6.6)	6 lots (462 units)
Latch-Up	Electrical	JESD78 (±200 mA)	2 lots
ESD	Human Body Model	JEDEC-JS001-2014	2 lots

(1) HAST – Highly accelerated temperature/humidity stress test
(2) HTOL – High temperature operation life

