RR120 & RR121 Digital Sensor Series
RR111 Analog Sensor Series

PRODUCT QUALIFICATION REPORT

December 5, 2017

Summary

This report documents the qualification and test results for Coto Technology's RR120, RR111 and RR121 series of Sensor products.

The digital sensors are fabricated using Coto Technology's second generation TMR process and assembled in industry standard packages such as SOT23 and LGA-4.

All of the environmental tests were performed at an accredited independent testing lab.

In total, 4,924 devices were tested with a variety of qualification stress tests under various test conditions. There were zero failures. This report certifies that the RR120 and RR121 series are qualified.

Reference Documents

JESD47I:	Stress-Test-Driven Qualification of Integrated Circuits
JESD22-A113:	Preconditioning MLS1 and MLS3
JESD22-A103:	High Temperature Storage Life (HTSL)
JESD22-A104:	Temperature Cycling
JESD22-A108:	Temperature, Bias, and Operating Life (HTOL)
JESD22-A118:	Unbiased HAST
JESD22-A110:	Biased HAST
JEDEC-JS001-2014:	ESD

JESD78: Latch Up

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1. Product Tested

The sensor products are fabricated using Coto Technology's second generation TMR process and assembled in industry standard packages.

All tests are performed by an accredited independent testing lab.

In total, 4,924 devices were stressed with a variety of qualification tests under various test conditions. Of the devices tested, there were zero failures during qualification testing.

2. Definition of Qualification

The RR120, RR111 and RR121 series of products are defined as products meeting all of the following criteria:

- A single TMR process technology (TMR = magnetic field sensor process)
- The same design rules and process technology.

3. Qualification Test Plan

The product qualification test plan is outlined in Table 1. This plan is based on the guidelines of the JESD47I, *Stress-Test-Driven Qualification of Integrated Circuits*, published by JEDEC Solid State Technology Association.

Table 1 – List of Qualification Test

Test	Stress	Duration	Sample Size
Parametric Tests	Evaluate datasheet spec at 25°C	N/A	All devices used for qualification
Pre-Conditioning	Thermal, Mechanical for package integrity SOT & TO92 Packages LGA package	 MSL1 MSL3	 10 lots (4000 units) 2 lots (680 units)
Temperature Cycle	Thermal, Mechanical	(-55°C; +125°C) 3 cycles/hr 1000 cycles	12 lots (924 units)
Unbiased HAST	Thermal, Moisture	@130°C, RH 85% 96 hrs	12 lots (924 units)
Biased HAST	Bias, Thermal Moisture	VCC @4V @130°C, RH 85% 96 hrs	12 lots (924 units)
HTOL	Bias, Thermal	1000 hrs (See Bias Conditions in Table 5 of Section 6.5)	13 lots (1001 units)
High Temperature Storage	Thermal, Material relaxation	1000 hrs (See Static Bake Conditions in Table 6 of Section 6.6)	13 lots (1001 units)
Latch-Up	Electrical	JESD78 (+/-200 mA)	6 lots
ESD	Human Body Model	JEDEC-JS001-2014	6 lots

HAST – Highly accelerated temperature/humidity stress test
HTOL – High temperature operation life

4. Sampling Plan

Random samples were selected for product qualification as shown in Table 1. Sample size meets or exceeds the number of samples recommended by JESD47I standard. Seventy-seven (77) sample units per lot were used for each stress test with 5% LTPD.

5. Failure Criteria

A device failure is defined as a condition in which a stressed device can no longer meet its datasheet specifications or it has consequential physical damage attributed to an environmental test.

6. Summary of Qualification Test Results

A summary of qualification test results is provided in following sections.

6.1. Pre-Conditioning

A total of 4,000 devices were pre-conditioned using JESD22-A113 level-1 procedures. Another 680 devices were pre-conditioned using JESD22-A113-level-3 procedures. Preconditioning is performed on samples before they are subjected to package-related stress tests. The samples were exposed to thermally stressful conditions equivalent to thermal conditions experienced by units during board soldering.

Table 1.2 – *Preconditioning* Results

Wafer Lot	MSL Level	Sample Size	Devices failed	Test Outcome
T515224.7, 515224.19, T511095, T515224.1, T515224.20, T702388.13, T702388.3, T706957.10, T706494.19	1	4,000	0	Pass
T706949, T706957.5	3	680	0	Pass

All parts have passed the Pre-conditioning.

6.2. Temperature Cycling

A total of 924 devices were tested with temperature cycling. Temperature cycling stresses devices between -55°C to +125°C at 3 cycles per hour for 1,000 cycles. This test is used for analysis of package performance.

Table 2 – Temperature Cycling Results

Wafer Lot	Sample Size	No. of Cycles	Devices failed	Test Outcome
T515224.7	77	1000	0	Pass
T515224.19	77	1000	0	Pass
T511095	77	1000	0	Pass
T515224.1	77	1000	0	Pass
T515224.20	77	1000	0	Pass
T512071	77	1000	0	pass
T702388.13	77	1000	0	Pass
T702388.3	77	1000	0	Pass
T706957.10	77	1000	0	Pass
T706494.19	77	1000	0	Pass
T706949	77	1000	0	Pass
T706957.5	77	1000	0	Pass

All parts have passed the Temperature Cycling test.

6.3. Unbiased HAST Test (Highly Accelerated Temperature/Humidity Stress Test)

A total 924 devices were tested for HAST. The HAST is done at +130°C and 85% relative humidity for 96 hours. This test is used for analysis of package performance.

Table 3 – UHAST Results

Wafer Lot	Sample Size	Ambient	Devices failed	Test Outcome
T515224.7	77	130^0C, RH 85%	0	Pass
T515224.19	77	130^0C, RH 85%	0	Pass
T511095	77	130^0C, RH 85%	0	Pass
T515224.1	77	130^0C, RH 85%	0	Pass
T515224.20	77	130^0C, RH 85%	0	Pass
T512071	77	130^0C, RH 85%	0	Pass
T702388.13	77	130^0C, RH 85%	0	Pass
T702388.3	77	130^0C, RH 85%	0	Pass
T706957.10	77	130^0C, RH 85%	0	Pass
T706494.19	77	130^0C, RH 85%	0	Pass
T706949	77	130^0C, RH 85%	0	Pass
T706957.5	77	130^0C, RH 85%	0	Pass

All parts have passed the unbiased HAST test.

6.4. *Biased HAST Test (Biased Highly Accelerated Stress Test)*

A total 924 devices were tested on biased HAST. The HAST is done at +130°C and 85% relative humidity under 4.0 V bias for 96 hours. This test is used for analysis of package performance under extreme operating conditions.

Table 4 – Biased HAST Results

	Sample Size	Ambient	Devices failed	Test Outcome
T515224.7	77	130^0C, RH 85%	0	Pass
T515224.19	77	130^0C, RH 85%	0	Pass
T511095	77	130^0C, RH 85%	0	Pass
T515224.1	77	130^0C, RH 85%	0	Pass
T515224.20	77	130^0C, RH 85%	0	Pass
T512071	77	130^0C, RH 85%	0	Pass
T702388.13	77	130^0C, RH 85%	0	Pass
T702388.3	77	130^0C, RH 85%	0	Pass
T706957.10	77	130^0C, RH 85%	0	Pass
T706494.19	77	130^0C, RH 85%	0	Pass
T706949	77	130^0C, RH 85%	0	Pass
T706957.5	77	130^0C, RH 85%	0	Pass

All parts have passed the biased HAST test.

6.5.1 HTOL Test (High Temperature Operation Life Test)

A total of 1,001 devices were tested HTOL. This test is used for analysis of life time of the device under extreme operating conditions.

Table 5 – HTOL Results

Wafer Lot	Sample Size	No. of Hours	Devices failed	Test Outcome	Bias Condition
T515224.7	77	1000	0	Pass	4V @150C
T515224.19	77	1000	0	Pass	4V @150C
T511095	77	1000	0	Pass	4V @ 125C
T515224.1	77	1000	0	Pass	4V @ 125C
T515224.20	77	1000	0	Pass	4V @150C
T512071	77	1000	0	Pass	4V @150C
T702388.13	77	1000	0	Pass	4V @150C
T702388.21	77	1000	0	Pass	4V @150C
T702388.3	77	1000	0	Pass	4V @150C
T706957.10	77	1000	0	Pass	4V @150C
T706494.19	77	1000	0	Pass	4V @150C
T706949	77	1000	0	Pass	4V @125C
T706957.5	77	1000	0	Pass	4V @125C

All parts have passed the HTOL test.

6.5.2 Early Life Failure Rate

Total of 1,440 units of various lots were stressed with high temperature life stress conditions (4.O V, +150C) for 168 hours. These units all passed the electrical test following the stress, there are no failures.

6.6. High Temperature Storage Test

A total of 1,001 devices were tested on high temperature storage. This test is used for analysis of device performance.

Table 6 – High Temperature Storage Results

Wafer Lot	Sample Size	No. of Hours	Devices failed	Test Outcome	Bake Temperature
T515224.7	77	1000	0	Pass	150C
T515224.19	77	1000	0	Pass	150C
T511095	77	1000	0	Pass	125C
T515224.1	77	1000	0	Pass	125C
T515224.20	77	1000	0	Pass	150C
T512071	77	1000	0	Pass	150C
T702388.13	77	1000	0	Pass	150C
T702388.21	77	1000	0	Pass	150C
T702388.3	77	1000	0	Pass	150C
T706957.10	77	1000	0	Pass	150C
T706494.19	77	1000	0	Pass	150C
T706949	77	1000	0	Pass	125C
T706957.5	77	1000	0	Pass	125C

All parts have passed the high temperature storage test.

6.7. ESD (HBM)

Human Body Model test was performed on a number of samples from three different lots of RR120, RR111 and RR121 series to characterize the susceptibility of devices to damage from electrostatic discharge (ESD) induced by human handling. Resulting data did not show any notable change due to ESD. Product is qualified for 4kV per JEDEC-JS001-2014.

6.8. Latch-up (LU)

Latch up characterization was successfully completed on samples from three different lots of RR120, RR111 and RR121 series using excessive current flow between the power supply and ground as well as output to power pin and to ground. Product is qualified per JESD78.

7. Conclusion

The RR120, RR111 and RR121 series products were tested as described in this report. The products tested met all electrical performance requirements and no failures were observed in any of the qualification tests. Based on these results, Coto Technology certifies that RR120, RR111 and RR121 series products are qualified.

Revision History:

Version	Date	Description
1.1	12/5/2016	Initial Release
1.2	7/7/2017	Added 2 more HTOL lots' data
1.3	9/22/2017	Added RR111 / RR121 series
1.4	12/5/2017	Completed RR111 / RR121 series