PRODUCT QUALIFICATION REPORT
RR120 and RR121 Digital Sensor Series
RR111 Analog Sensor Series

Test	Stress	Duration	Sample Size
Parametric Tests	Evaluate datasheet spec at 25°C	N/A	All devices used for qualification
Pre-Conditioning	Thermal, Mechanical for package integrity SOT & TO92 Packages LGA package	 MSL1 MSL3	 10 lots (4000 units) 2 lots (680 units)
Temperature Cycle	Thermal, Mechanical	(-55°C; +125°C) 3 cycles/hr 1000 cycles	12 lots (924 units)
Unbiased HAST	Thermal, Moisture	@130°C, RH 85% 96 hrs	12 lots (924 units)
Biased HAST	Bias, Thermal Moisture	VCC @4V @130°C, RH 85% 96 hrs	12 lots (924 units)
HTOL	Bias, Thermal	1000 hrs (See Bias Conditions in Table 5 of Section 6.5)	13 lots (1001 units)
High Temperature Storage	Thermal, Material relaxation	1000 hrs (See Static Bake Conditions in Table 6 of Section 6.6)	13 lots (1001 units)
Latch-Up	Electrical	JESD78 (+/-200 mA)	6 lots
ESD	Human Body Model	JEDEC-JS001-2014	6 lots

HAST – Highly accelerated temperature/humidity stress test
HTOL – High temperature operation life

** This plan is based on the guidelines of the JESD47I, Stress-Test-Driven Qualification of Integrated Circuits, published by JEDEC Solid State Technology Association.*